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09/923,997	08/07/2001	Hiroyuki Takahashi	SIM-01501	1911

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EXAMINER	
TRA, ANH QUAN	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 10/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,997	TAKAHASHI, HIROYUKI	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,19-24 and 27-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,19-24 and 27-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 08/19/04. The allowable subject matters of claims 15 and 22-24 have been withdrawn. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Takashima (JP 06-208790).

Takashima discloses in figure 8 a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: an inverter chain containing not less than four inverters; a p-channel metal-oxide-semiconductor transistor and an n-channel metal-oxide-semiconductor transistor, known as MOS transistors, to comprise each of the at least four inverters, wherein a gate threshold voltage of each gate is shifted in mutually opposing directions; low threshold voltage n-MOS transistors (Qn1, Qn3) of each of a first and a third inverter connected to ground by a high threshold voltage n-MOS transistor (Qn5 in figure 10a); and low threshold voltage P-MOS transistors (Qp2, Qp4) of each of a second and a fourth inverter connected to ground by a high threshold voltage P-MOS transistor (Qp5); wherein, when an input logic signal is fixed at a low level during a standby state, the high threshold voltage n-MOS transistor is set to an off-state in response to a chip select signal (Φ1)controlling the standby state, and the high threshold voltage P-MOS transistor is set to an off-state in response to

the chip select signal that is negated (further see figure 12 and column 3, line 45 and column 4, line 60 of USP 6414363 which describe the detail and operation of Takashima's figure 8).

3. Claims 20, 27, 28 and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (USP 5825698).

As to claim 20, Kim et al discloses in figure 3 a delay circuit, comprising: first and second nodes (node between 48 and 50 and node between 50 and 51); a first inverter (48), the output of which coupled to the first node, the first inverter receiving a logic signal; a second inverter (50), the input of which coupled to the first node and the output of which coupled to the second node; a first capacitor (49) coupled between the first node and a first power source line, the first capacitor being a first transistor of a first channel type (p-type); and a second capacitor (52) coupled between the second node and a second power source line which is different from the first power source line, the second capacitor being a second transistor of a second channel type (n-type) which is different from said first channel type; wherein the first transistor is a P-MOS transistor, the second transistor is an n-MOS transistor, and the second power source line is a fixed at a ground potential.

As to claim 27, figure 3 shows a delay circuit receiving a logic signal having a first logical level and a second logical level, comprising: an inverter chain (48-62) including a plurality of inverters and at least one first capacitor (49), the inverter chain receiving the logic signal, the first capacitor including a MOS transistor of a first channel type (p-type), the first capacitor being operated so that the capacitor changes in off-state to on-state (when signal at node N1 changed from low state to high state) to increase its capacitance when the logic signal changes from the first logical level (low) to the second logical level (high), whereby the inverter

chain outputs a first delay signal generated after a first delay time from the transition timing from the first to the second logical levels of the logic signal, the first capacitor being operated so that the capacitor changes in the on-state to the off-state to decrease its capacitance when the logic signal changes from the second logical level to the first logical level, whereby the inverter chain outputs a second delay signal generated after a second delay time from the transition timing from the second to the first logical levels of the logic signal, the second delay time being shorter than the first delay time (inherent. Further see the timing diagram of nodes 502-507 in figure 2 of USP 6037815), a logical gate (63) receiving the output of the inverter chain and the logic signal so that the logical gate outputs its output signal in response to the first delay signal when the logic signal changes from the first logical level to the second logical level.

As to claim 28, figure 3 shows a second capacitor (52), the second capacitor being comprised of an MOS transistor of a second channel type (n-type) which is different from the first channel type, the second capacitor being coupled to a node which is different from the node coupled to the first capacitor in the inverter chain, the second capacitor being operated so that the capacitor changes in off-state to on-state to increase its capacitance when the logic signal changes from the first logical level to the second logical level, whereby the inverter chain outputs a first delay signal generated after a first delay time from the transition timing from the first to the second logical levels of the logic signal, the second capacitor being operated so that the capacitor changes in the on-state to the off-state to decrease its capacitance when the logic signal changes from the second logical level to said first logical level, whereby the inverter chain outputs a second delay signal generated after a second delay time from the transition timing from

the second to the first logical levels of the logic signal, the second delay time being shorter than the first delay time (inherent).

As to claim 31, Kim et al.'s figure 3 shows a delay circuit, comprising: 2n+1 nodes defined in series, n being a natural number (n=4), a first node (N1) receiving a logical signal; 2n inverters (48-62), each inverter arranged between adjacent nodes of the 2n+1 nodes; a capacitor (47, 52, 55, 59) of an n-MOS type coupled between an odd node and a first power source line (ground); a capacitor (49, 53, 57, 61) of a P-MOS type coupled between an even node and a second power source line; and a NAND gate coupled to the first node and the (2n+1)th node.

4. Claims 22 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by McClure (USP 5115146).

As to claim 22, McClure discloses in figure 1 a delay circuit (circuit comprises elements 12), comprising: first, second and third nodes; a first inverter (the second inverter from the left), the output of which coupled to the first node, the first inverter receiving a logic signal; a second inverter (the third inverter from the left), the input of which coupled to the first node and the output of which coupled to the second node; a third inverter (the fourth inverter from the left), the input of which coupled to the second node and the output of which coupled to the third node; a fourth inverter (the fifth inverter from the left), the input of which coupled to the third node; a first capacitor coupled between the first node and a first power source line (VCC), first capacitor being a first transistor of a first channel type (p-type); a second capacitor coupled between the third node and the first power source line, the second capacitor being a second transistor of the first channel type; and wherein no capacitor is connected to the second node.

As to claim 23, figure 1 shows that the first transistor and the second transistor are P-MOS transistors, and the first power source line is fixed at a power potential.

5. Claims 22 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (USP 5055713) (previously cited).

As to claim 22, Watanabe et al. discloses in figure 11 a delay circuit (I9-I11 and NG), comprising: first, second and third nodes; a first inverter (I9), the output of which coupled to the first node, the first inverter receiving a logic signal; a second inverter (I10), the input of which coupled to the first node and the output of which coupled to the second node; a third inverter (I11), the input of which coupled to the second node and the output of which coupled to the third node; a fourth inverter (NG), the input of which coupled to the third node; a first capacitor (C2) coupled between the first node and a first power source line (Vss), first capacitor being a first transistor of a first channel type (n-type); a second capacitor (C3) coupled between the third node and the first power source line, the second capacitor being a second transistor of the first channel type; and wherein no capacitor is connected to the second node.

As to claim 24, figure 11 shows that the first transistor and the second transistor are n-MOS transistors, and the first power source line is fixed at a ground potential.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takashima (JP 06-208790) in view of Kim et al. (USP 5825698).

As to claim 19, Takashima's figure 8 shows all limitations of the claim except for first capacitor coupled between a first node and the power source, and a second capacitor coupled between the second node and a second power source. However, Kim et al.'s figure 3 shows a delay chain (48-62) having capacitors alternately and respectively coupled the nodes of the delay chain to power supply and ground in order to further delay the rising edge or the falling edge of the input signal. therefore, it would have been obvious to one having ordinary skill in the art to employ Kim et al.'s teaching for Takashima's delay circuit for the purpose of further delay the positive or negative edge of the input signal.

As to claim 21, the location of the capacitors determined which edge (positive of negative) of the input signal is to be further delay. Therefore, it would have been obvious to one having ordinary skill in the art to select the first capacitor is n-MOS transistor and the second capacitor is P-MOS transistor for the purpose of further delay the negative edge of the input signal.

8. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chaw (USP 5672990).

Claw's figure 5 shows a delay circuit, comprising 2n+1 nodes (n=1; input node, ode between 30a, 30b, and node between 30b and 30c) defined in series, n being a natural number (n=1), a first node receiving a logical signal (input); 2n inverters (30a, 30b), each inverter arranged between adjacent nodes of the 2n+1 nodes; a capacitor coupled between an even node and a power source line (ground); and a NOR gate (30c) coupled to the first node and the

(2n+1)th node. Thus, figure 5 shows all limitations of the claim except for the capacitor is NMOS transistor. However, it is notoriously well known that MOS capacitor is more compact than regular capacitor. Therefore, it would have been obvious to one having ordinary skill in the art to use NMOS transistor connected as capacitor for Chaw's capacitor for the purpose of saving space.

9. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (USP 5825698).

Kim et al.'s figure 3 shows a delay circuit, comprising: 2n+1 nodes defined in series, n being a natural number (n=4), a first node (N1) receiving a logical signal; 2n inverters (48-62), each inverter arranged between adjacent nodes of the 2n+1 nodes; a capacitor (47, 52, 55, 59) of an n-MOS type coupled between an odd node and a first power source line (ground); a capacitor (49, 53, 57, 61) of a P-MOS type coupled between an even node and a second power source line; and a NAND gate coupled to the first node and the (2n+1)th node. Kim et al. fails to show an AND gate coupled to the first node and the (2n+1)th node. However, it notoriously well known in the art that NAND gate is equivalent to an AND gate coupled in series with an inverter. Therefore, it would have been obvious to one having ordinary skill in the art to replace NAND gate 63 with AND gate coupled in series with an inverter due to doctrine equivalent of function.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Patent Examiner

October 25, 2004